REMARKS

This Amendment is submitted in response to the Office Action of May 2, 2006 (hereinafter "the Office Action"). Upon entry of this Amendment, claims 5, 9, 11, and 15 will be canceled without prejudice, claims 1-4, 6-8, 10, 12-14, and 16-20 amended, and no new claims submitted. Therefore claims 1-4, 6-8, 10, 12-14, and 16-20 will be pending.

All references to the claims, except as noted, will be made with reference to the claim list above beginning on page 3. All references to "the Office Action," except as noted, will be referencing the most recent Office Action dated May 2, 2006. Line numbers referenced in the Office Action, except as noted, will count every printed line, except the page header, but including section headings. If there is any confusion or questions regarding any aspect of this Amendment, the Examiner is invited to contact the undersigned.

Amendment

Claim 1 was amended to specify that the integer execution unit operates at the CPU clock signal frequency while the floating point graphics unit operates at a second frequency which is a multiple of the first frequency. Support for these changes can be found in paragraphs 25-27 of the original specification. In addition, claim 1 now cites a plurality of latches and a merge unit. These elements are shown in Figure 4, and described in paragraphs 27 and 28. Claim 1 was further amended to provide that the floating point graphics unit performs floating point arithmetic operations (claim 1, lines 17-18). Support for this change can be found in paragraph 4 of the specification as filed.

Claims 2-4 and 6-13 were amended in the preamble for grammar by replacing "A processor of claim X" with "*The* processor of claim X" (emphasis added). In addition, claims 2 and 4 were amended for improved readability.

Claims 5, 9, 11, and 16 are canceled without prejudice.

Claim 14 was generally amended to functionally tie the various elements together. In addition, to improve clarity, the preamble of claim 14 is changed from "A circuit, comprising: a floating point graphics unit . . . having," to "A floating point graphics unit . . . comprising:". Claim 14 now sets forth "a plurality of pulse generators" which are shown at 620 in Figure 6 and discussed in paragraph 33 of the specification.

Claims 16-18 are amended so that the preambles are consistent with the independent claim and for improved consistency with the independent claim.

Claim 19 is amended to better functionally tie the elements together. Claim 20 was amended for consistency with claim 19.

No new matter has been entered by this Amendment.

Claim Objections

Claim 11 is objected to for being a duplicate of claim 6. Claim 11 is amended to depend from claim 7 instead of from claim 2, thereby obviating this Objection.

Claim Rejections - 35 U.S.C. § 103(a)

Claims 1-20 stand rejected under 35 U.S.C. § 103(a) for being unpatentable over various combinations of:

(1) "Applicants Admitted Prior Art," hereinafter "AAPA";

(2) U.S. Patent 6,477,221 to Ning, hereinafter, "Ning";

(3) U.S. Patent 6,177,844 to Sung et al., hereinafter, "Sung"; and

(4) U.S. Patent 6,950,488 to Chung et al., hereinafter "Chung".

Applicant respectfully traverses.

It is initially noted that the Office Action appears to take judicial notice that it was well known to have a delay-locked loop circuit in a processor to generate a multiple of a processor clock signal (Office Action, page 5, lines 2-4 and 14-16; page 6, lines 7-9; page 7, lines 2-4 and 14-16; page 8, lines 6-8, page 9, lines 2-4; page 10, lines 7-9; and page 11, lines 2-4 and 13-15). Applicant respectfully disagrees and submits that the conclusory statements by the Office are inappropriate. "It would not be appropriate for the examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well-known" (MPEP 2144.03.A) (emphasis in original). Applicant therefore respectfully requests proof of the statements that it was well known to have a delay-locked loop circuit in a processor to generate a multiple of a processor clock signal.

Ning is cited with respect to claims 1-13, 19, and 20 for showing having a single floating point unit corresponding to a plurality of integer units (Office Action, page 3, lines 8-

10 and page 13, lines 14-15). However, claim 1 now sets forth that the integer units generate an output signal at a first frequency, that a plurality of latches are connected to receive output signals from the integer execution units, that a merge unit generating a merged signal containing the output signals at a second frequency that is a multiple of the first frequency, and that the floating point graphics unit processes the merged signal at the second frequency (claim 1, lines 9-17). In addition, claim 19, from which claim 20 depends, now provides a combined custom clock signal having a frequency that is a multiple of the frequency of the CPU clock signal. These features are neither taught nor suggested by Ning and the other cited art of record.

Sung is cited with respect to claims 2-10 and 14-20 for showing a delay-locked loop circuitry usable in clock signal distribution networks and a charge-pump circuit (Office Action, page 4, lines 11-14; page 5, lines 4-7; page 5, line 15 to page 6, line 1; page 6, lines 9-12; page 7, lines 4-8; page 7, line 14-19; page 8, lines 8-13; page 9, lines 4-7; page 10, lines 9-11; and page 11, lines 4-7 and lines 15-18). With regard to independent claim 14, Sung is also cited for showing a delay-locked loop circuit usable in the clock signal distribution networks of programmable logic devices, a voltage control delay line unit, a phase frequency detector, a charge pump, at least one symmetric NOR at least one symmetric NAND, and a buffer (page 10, lines 11-14). However, claim 2 now sets forth that a DLL circuit "capable of generating a clock signal at the second frequency" (claim 2, lines 3-4) which is a multiple of the first frequency (claim 1, lines 14-15). Claim 12 states that the higher frequency clock has a higher frequency than the CPU clock signal and independent claim 19 now specifies that the combined custom clock signal has a frequency that is a multiple of the CPU clock signal. Independent claim 14 now requires that the various elements be connected in a functionally specific way. For example, claim 14 sets forth a phase frequency detector "capable of detecting the phase difference between the first signal and the last [delayed clock signal] signal" (claim 14, lines 9-10).

Chung is cited for showing a Schmitt circuit in a delay-locked loop circuit (Office Action, page 9, lines 16-17). However, Chung relates to a delay-locked loop circuit that synchronizes an internal clock with an external clock (col. 1, lines 10-15). Chung does not cure the deficiencies of Sung and Ning described above.

For a rejection under 35 U.S.C. § 103(a), each and every claim limitation must be taught or suggested by the prior art. Since the prior art of record does not teach or suggest the

claimed invention as set forth in any of the pending claims, Applicant respectfully submits that the application is in condition for Allowance. A notice of Allowance is therefore respectfully requested.

If the Examiner has any questions concerning the present amendment, the Examiner is kindly requested to contact the undersigned at (408) 774-6933. If any other fees are due in connection with filing this amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. SUNMP348). A duplicate copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
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